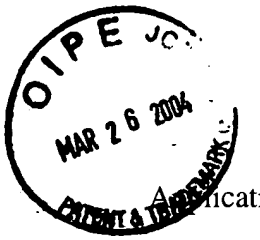
03-29-04




Express Mail No.: EV 371 773 015 US

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Application of: | Donnelly, Kevin S. | Confirmation No.: | Not yet assigned |
| Serial No.: | 10/699,116 | Art Unit: | Not yet assigned |
| Filed: | October 31, 2003 | Examiner: | Not yet assigned |
| For: | Transceiver with Latency Alignment Circuitry | Attorney Docket No: | 060809-0143-US (formerly 9797-0143-999) |

TRANSMITTAL OF POWER OF ATTORNEY BY ASSIGNEE
REVOKING PREVIOUS POWERS OF RECORD

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants' attorney encloses herewith a Revocation and Power of Attorney by Assignee with Certification Under 3.73(b) for the above identified application.

Please change the attorney docket number to 060809-0143-US. Future correspondence should be forwarded to customer no. **38426**.

The Commissioner is authorized to charge any fees associated with this communication to Morgan, Lewis & Bockius LLP deposit account no. 50-0310 (order no. 060809-0143-US). A copy of this sheet is enclosed for such purpose.

Respectfully submitted,

Date: 3/26/04

Gary S. Williams 31,066
(Reg. No.)

**MORGAN, LEWIS & BOCKIUS** LLP
2 Palo Alto Square
3000 El Camino Real, Suite 900
Palo Alto, California 94306
(650) 493-4935

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: See Attached Schedule A

Serial No.: See Attached Schedule A

Filed: See Attached Schedule A

For: See Attached Schedule A

REVOCATION AND POWER OF ATTORNEY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S I R:

Rambus Inc., owner of the entire right, title and interest in, to and under the invention described and claimed in the above-identified patent application hereby revokes all previous powers of attorney and appoints Morgan, Lewis & Bockius LLP, customer no. 38426, and each of them, its attorneys, to prosecute this application, and to transact all business in the Patent and Trademark Office connected therewith.

In addition, the undersigned assignee also appoints Paul M. Anderson (Reg. No. 39,896), Paula J. Lagattuta (Reg No. 40,691), Jose G. Moniz ( Reg. 50,192) and Kent R. Richardson (Reg. No. 39,443) of Rambus Inc., to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Please direct all future correspondence to Customer Number 38426, Morgan, Lewis & Bockius LLP, located at 3300 Hillview Avenue, Palo Alto, California 94304, and direct all telephone calls to Morgan, Lewis & Bockius LLP at (650) 493-4935.

Date: 2/24/04

Assignee: Rambus Inc.
Signature:
Typed Name: Kent R. Richardson
Position/Title: Vice President, Intellectual Property
Address: 4440 El Camino Real
Los Altos, CA 94022


# SCHEDULE A

## [U.S.]

| Serial No:/Patent No: | Filing Date/Issue Date: | Title: | 1st Named Inventor: | Docket No: |
|---|---|---|---|---|
| 09/271,611; 6,125,422 | March 17, 1999; September 26, 2000 | Dependent Bank Memory Controller Method And Apparatus | May, Bradley A. | 60809-0003 |
| 09/346,682; 6,453,401 | July 2, 1999; September 17, 2002 | Memory Controller With Timing Constraint Tracking and Checking Unit and Corresponding Method | Barth, Richard M. | 60809-0004 |
| 60/061,664 | October 10, 1997 | Power Control System For Synchronous Memory Device | Tsern, Ely K. | 60809-0006PV |
| 09/169,378; 6,263,448 | October 9, 1998; July 17, 2001 | Power Control System For Synchronous Memory Device | Tsern, Ely K. | 60809-0006 |
| 60/061,682 | October 10, 1997 | Pipelined Memory Device | Barth, Richard M. | 60809-0008PV |
| 09/169,526; 6,356,975 | October 9, 1998; March 12, 2002 | Apparatus and Method For Pipelined Memory Operations | Barth, Richard M. | 60809-0008 |
| 60/034,436 | December 23, 1996 | Redundancy For Wide Hierarchical I/O Organization | Stark, Donald C. | 60809-0009PV |
| 08/970,053 ABANDONED | November 13, 1997 | Redundancy For Wide Hierarchical I/O Organizations | Stark, Donald C. | 60809-0009 |
| 60/062,035 | October 10, 1997 | Gear Ratio Techniques and Distributed Clock Generation | Ware, Frederick A. | 60809-0010PV |
| 09/169,589; 6,396,887 | October 9, 1998; May 28, 2002 | Apparatus and Method For Generating a Distributed Clock Signal Using Gear Ratio Techniques | Ware, Frederick A. | 60809-0010 |

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|---|---|---|---|---|
| 60/061,503 | October 10, 1997 | Two Steps Writes | Davis, Paul G. | 60809-0011PV |
| 09/169,736; 6,343,352 | October 9, 1998; January 29, 2002 | Method and Apparatus For Two Step Memory Write Operations | Davis, Paul G. | 60809-0011 |
| 60/061,769 | October 10, 1997 | Device Timing Compensation | Ware, Frederick A. | 60809-0015PV |
| 09/169,687; 6,226,754 | October 09, 1998; May 1, 2001 | Apparatus and Method For Device Timing Compensation | Ware, Frederick A. | 60809-0015 |
| 60/061,770 | October 10, 1997 | High Performance Cost Optimized Memory | Barth, Richard M. | 60809-0016PV |
| 09/169,206; 6,401,167 | October 9, 1998; June 4, 2002 | High Performance Cost Optimized Memory | Barth, Richard M. | 60809-0016 |
| 60/063,471 | October 10, 1997 | Techniques For Maximizing Information Transferred Over Limited Interconnect Resources in Electronic Systems | Abhyankar, Abhijitm | 60809-0017PV |
| 09/169,748; 6,347,354 | October 9, 1998; February 12, 2002 | Apparatus and Method For Maximizing Information Transfers Over Limited Interconnect Resources | Abhyankar, Abhijit M. | 60809-0017 |
| 08/795,657; 6,125,157 | February 6, 1997; September 26, 2000 | Delay-Locked Loop Circuitry For Clock Delay Adjustment | Donnelly, Kevin S. | 60809-0018 |
| 60/061,505 | October 10, 1997 | Method and Apparatus For Fail-Safe Resynchronization With Minimum Latency | Zerbe, Jared L. | 60809-0019PV |
| 09/169,372; 6,473,439 | October 9, 1998; October 29, 2002 | Method and Apparatus For Fail-Safe Resynchronization With Minimum Latency | Zerbe, Jared L. | 60809-0019 |
| 09/306,897; 6,426,984 | May 7, 1999; July 30, 2002 | Apparatus and Method For Reducing Clock Signal Phase Skew in a Master-Slave System With Multiple Latent Clock Cycles | Perino, Donald V. | 60809-0020 |

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|---|---|---|---|---|
| 09/353,547 | July 14, 1999 | Apparatus and Method For Controlling A Master/Slave System Via Master Device Synchronization | Sidiropoulos, Stefanos | 60809-0022 |
| 60/219,358; 6,523,089 | July 19, 2000; February 18, 2003 | Memory Controller With Power Management Logic | Tsern, Ely K. | 60809-0024PV |
| 09/907,338; 6,523,089 | July 16, 2001; February 18, 2003 | Memory Controller With Power Management Logic | Tsern, Ely K. | 60809-0024 |
| 08/904,203; 5,945,862 | July 31, 1997; August 31, 1999 | Circuitry For the Delay Adjustment of a Clock Signal | Donnelly, Kevin S. | 60809-0025 |
| 09/245,140 | February 4, 1999 | Spread Spectrum Clocking of Digital Signals | Perino, Donald V. | 60809-0026 |
| 09/471,305; 6,404,660 | December 23, 1999; June 11, 2002 | Semiconductor Package With a Controlled Impedance Bus and Method of Forming Same | Gamini, Nader | 60809-0027 |
| 09/358,054; 6,232,796 | July 21, 1999; May 15, 2001 | Apparatus and Method For Detecting Two Data Bits Per Clock Edge | Batra, Pradeep | 60809-0029 |
| 60/061,767 | October 10, 1997 | Dram Core Refresh With Reduced Overhead | Tsern, Ely K. | 60809-0030PV |
| 09/169,376; 6,075,744 | October 9, 1998; June 13, 2000 | Dram Core Refresh With Reduced Spike Current | Tsern, Ely K. | 60809-0030 |
| 09/222,590; 6,163,178 | December 28, 1998; December 19, 2000 | Impedance Controlled Output Driver | Stark, Donald C. | 60809-0031 |
| 08/897,658; 6,205,191 | July 21, 1997; March 20, 2001 | Method and Apparatus For Synchronizing a Control Signal | Portmann, Clemenz | 60809-0032 |
| 08/938,084; 6,067,594 | September 26, 1997; May 23, 2000 | High Frequency Bus System | Perino, Donald V. | 60809-0033 |

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|---|---|---|---|---|
| 60/057,900 | September 5, 1997 | Small-Swing to CMOS Conversion Circuit With Duty Cycle Correction | Portmann, Clemenz | 60809-0034PV |
| 09/146,286; 6,169,434 | September 3, 1998; January 2, 2001 | Conversion Circuit With Duty Cycle Correction For Small Swing Signals, and Associated Method | Portmann, Clemenz L. | 60809-0034 |
| 60/057,400 | August 29, 1997 | Current Control Technique | Garrett, Jr., Billy Wayne | 60809-0035PV |
| 09/141,675; 6,094,075 | August 27, 1998; July 25, 2000 | Current Control Technique | Garrett, Jr., Billy Wayne | 60809-0035 |
| 09/025,983; 6,014,042 | February 19, 1998; January 11, 2000 | Phase Detector Using Switched Capacitors | Nguyen, Nhat M. | 60809-0036PV |
| 09/179,139; 6,198,307 | October 26, 1998; March 6, 2001 | Output Driver Circuit With Well-Controlled Output Impedance | Garlepp, Bruno Werner | 60809-0039 |
| 60/061,674 | October 10, 1997 | Method And Apparatus For Two-Step Memory Write Operations | Davis, Paul G. | 60809-0041PV |
| 60/061,692 | October 10, 1997 | Technical Description Version 0.1 | Barth, Richard M. | 60809-0042PV |
| 60/061,697 | October 10, 1997 | Marketing Collateral | Barth, Richard M. | 60809-0043PV |
| 60/061,783 | October 10, 1997 | Technical Description Version 0.6 | Barth, Richard M. | 60809-0044PV |
| 60/062,014 | October 10, 1997 | Technical Description Version 0.5 | Barth, Richard M. | 60809-0045PV |
| 60/033,889 | December 26, 1996 | Shared Sense AMP Dram Cores | Barth, Richard M. | 60809-0046PV |
| 60/038,901 | February 28, 1997 | Low-Latency Small-Swing Clocked Receiver | Zerbe, Jared L. | 60809-0047PV |
| 08/896,934; 5,977,798 | July 18, 1997; November 2, 1999 | Low-Latency Small-Swing Clocked Receiver | Zerbe, Jared L. | 60809-0047 |
| 60/039,612 | March 12, 1997 | Method of Source Coding With Inherent Clock Synchronization | Perino, Donald V. | 60809-0048PV |
| 60/073,353 | February 2, 1998 | Current Control Circuit | Garrett, Jr. Billy Wayne | 60809-0049PV |

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|---|---|---|---|---|
| 09/478,916 | January 6, 2000 | Low Latency Multi-Level Communication Interface | Zerbe, Jared L. | 60809-0050 |
| 09/706,238 | November 2, 2000 | Expandable Slave Device System | Garlepp, Bruno W. | 60809-0051 |
| 09/291,091; RE36,781 | April 13, 1999; July 18, 2000 | Differential Comparator For Amplifying Small Swing Signals to a Full Swing Output | Lee, Thomas H. | 60809-0052 |
| 60/158,189 | October 19, 1999 | A Method and Apparatus For Receiving High Speed Signals With Low Latency | Zerbe, Jared L. | 60809-0053PV |
| 09/478,914; 6,396,329 | January 6, 2000; May 28, 2002 | A Method and Apparatus For Receiving High-Speed Signals With Low Latency | Zerbe, Jared L. | 60809-0053 |
| 09/398,252; 6,122,208 | September 17, 1999; September 19, 2000 | Circuit and Method For Column Redundancy For High Bandwidth Memories | Stark, Donald C. | 60809-0054 |
| 09/513,721; 6,323,706 | February 24, 2000; November 27, 2001 | Apparatus and Method For Edge Based Duty Cycle Conversion | Stark, Donald C. | 60809-0055 |
| 09/467,446; 6,657,468 | December 20, 1999; December 2, 2003 | Apparatus and Method For Controlling Edge Rates of Digital Signals | Best, Scott C. | 60809-0056 |
| 09/629,862 | August 1, 2000 | Apparatus and Method For Operating a Master-Slave System With a Clock Signal and a Separate Phase Signal | Perino, Donald V. | 60809-0057 |
| 09/579,776; 6,621,373 | May 26, 2000; September 16, 2003 | Apparatus and Method For Utilizing a Lossy Dielectric Substrate in a High Speed Digital System | Mullen, Donald R. | 60809-0059 |
| 09/633,961; 6,504,448 | August 8, 2000; January 7, 20030 | Apparatus and Method For Transmission Line Impedance Tuning Using Periodic Capacitive Stubs | Yip, Wai-Yeung | 60809-0060 |

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|---|---|---|---|---|
| 09/420,949; 6,321,282 | October 19, 1999; November 20, 2001 | Apparatus and Method For Topography Dependent Signaling | Horowitz, Mark A. | 60809-0061 |
| 09/390,217 ABANDONED | September 3, 1999 | High Performance Cost Optimized Memory With Delayed Memory Writes | Barth, Richard M. | 60809-0062 |
| 09/390,218; 6,204,697 | September 3, 1999; March 20, 2001 | Low-Latency Small-Swing Clocked Receiver | Zerbe, Jared L. | 60809-0063 |
| 09/507,302 | February 18, 2000 | System Having Both Externally and Internally Generated Clock Signals Being Asserted on the Same Clock Pin in Normal and Test Modes of Operation Respectively | Lau, Benedict C. | 60809-0064 |
| 09/564,064; 6,449,159 | May 3, 2000; September 10, 2002 | Semiconductor Module With Imbedded Heat Spreader | Haba, Belgacem | 60809-0065 |
| 09/507,303; 6,266,730 | February 18, 2000; July 24, 2001 | High-Frequency Bus System | Perino, Donald V. | 60809-0066 |
| 09/524,402; 6,539,072 | March 13, 2000; March 25, 2003 | Delay-Locked Loop Circuitry For Clock Delay Adjustment | Donnelly, Kevin S. | 60809-0067 |
| 09/561,603; 6,266,292 | April 27, 2000; July 24, 2001 | Dram Core Refresh With Reduced Spike Current | Tsern, Ely K. | 60809-0068 |
| 09/561,592; 6,343,042 | April 27, 2000; January 29, 2002 | Dram Core Refresh With Reduced Spike Current | Tsern, Ely K. | 60809-0069 |
| 09/792,788 | February 22, 2001 | Stacked Semiconductor Module | Fox, Thomas F. | 60809-0070 |
| 09/685,941; 6,376,904 | October 10, 2000; April 23, 2002 | Redistributed Bond Pads in Stacked Integrated Circuit Die Package | Haba, Belgacem | 60809-0071 |

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|---|---|---|---|---|
| 09/665,731; 6,282,604 | September 20, 2000; August 28, 2001 | Dependent Bank Memory Controller Method And Apparatus | May, Bradley A. | 60809-0072 |
| 10/071,298 | February 7, 2002 | Semiconductor Module With Serial Bus Connection to Multiple Dies | Haba, Belgacem | 60809-0074 |
| 09/038,353 **ABANDONED** | March 10, 1998 | Performing Concurrent Refresh and Current Control Operations in a Memory Subsystem | Hampel, Craig E. | 60809-0075 |
| 09/637,892; 6,310,814 | August 8, 2000; October 30, 2001 | Dram Apparatus and Method For Performing Refresh Operations | Hampel, Craig E. | 60809-0076 |
| 09/698,997; 6,342,800 | October 26, 2000; January 29, 2002 | Charge Compensation Control Circuit and Method For Use With Output Driver | Stark, Donald C. | 60809-0077 |
| 09/699,325; 6,594,326 | October 27, 2000; July 15, 2003 | Apparatus and Method For Synchronizing a Control Signal | Portmann, Clemenz | 60809-0078 |
| 09/800,552; 6,448,813 | March 6, 2001; September 10, 2002 | Output Driver Circuit With Well-Controlled Output Impedance | Garlepp, Bruno W. | 60809-0079 |
| 09/839,768 | April 19, 2001 | High-Frequency Bus System | Liaw, Haw-Jyh | 60809-0080 |
| 10/087,395 | March 1, 2002 | Semiconductor Module | Haba, Belgacem | 60809-0081 |
| 10/098,520 | March 13, 2002 | Memory Module | Haba, Belgacem | 60809-0082 |
| 09/887,181 | June 21, 2001 | Power Control System For Synchronous Memory Device | Tsern, Ely K. | 60809-0083 |
| 09/910,217; 6,516,365 | July 19, 2001; February 4, 2003 | Apparatus and Method For Topography Dependent Signaling | Horowitz, Mark A. | 60809-0084 |
| 10/014,457 | December 11, 2001 | Memory System and Method For Two Step Write Operations | Davis, Paul G. | 60809-0085 |
| 10/053,632 | January 18, 2002 | Apparatus and Method For Pipelined Memory Operations | Barth, Richard M. | 60809-0086 |

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| 09/978,278; 6,448,828 | October 15, 2001; September 10, 2002 | Apparatus and Method For Edge Based Duty Cycle Conversion | Stark, Donald C. | 60809-0087 |
| 10/014,650; 6,661,268 | December 11, 2001; December 9, 2003 | Charge Compensation Control Circuit and Method For Use With Output Driver | Stark, Donald C. | 60809-0088 |
| 09/421,073, 6,643,787 | October 19, 1999; November 4, 2003 | Bus System Optimization | Zerbe, Jared L. | 60809-0089 |
| 10/091,979 | March 4, 2002 | Apparatus and Method For Generating a Distributed Clock Signal Using Gear Ratio Techniques | Ware, Frederick A. | 60809-0090 |
| 10/045,864; 6,583,035 | January 9, 2002; June 24, 2003 | Semiconductor Package With a Controlled Impedance Bus and Method of Forming Same | Gamini, Nader | 60809-0091 |
| 10/072,412; 6,514,794 | February 5, 2002; February 4, 2003 | Redistributed Bond Pads in Stacked Integrated Circuit Die Package | Haba, Belgacem | 60809-0092 |
| 10/247,188 | September 19, 2002 | Multiple Sweep Point Testing of Circuit Devices | Chang, Timothy C. | 60809-0093 |
| 10/066,488 | January 30, 2002 | Apparatus and Method For Maximizing Information Transfers Over Limited Interconnect Resources | Abhyankar, Abhijit | 60809-0094 |
| 10/066,042; 6,597,616 | January 29, 2002; July 22, 2003 | Dram Core Refresh With Reduced Spike Current | Tsern, Ely K. | 60809-0095 |
| 10/123,370 | April 15, 2002 | Method and Apparatus For Receiving High Speed Signals With Low Latency | Zerbe, Jared L. | 60809-0096 |
| 60/376,947 | April 30, 2002 | Timing Calibration Apparatus and Method For a Memory Device Signaling System | Ware, Frederick A. | 60809-0097PV |

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|---|---|---|---|---|
| 10/278,478 | October 22, 2002 | Timing Calibration Apparatus and Method For a Memory Device Signaling System | Hampel, Craig E. | 60809-0097 |
| 60/498,511 | August 27, 2003 | Integrated Circuit Input/Output Interface With Empirically Determined Delay Matching | Hampel, Craig E. | 60809-0098PV |
| 10/676,648 | September 30, 2003 | Integrated Circuit With Bi-Modal Data Strobe | Hampel, Craig E. | 60809-0099 |
| 10/128,167 | April 22, 2002 | High Performance Cost Optimized Memory | Barth, Richard M. | 60809-0100 |
| 09/523,520; 6,530,062 | March 10, 2000; March 4, 2003 | Active Impedance Compensation | Liaw, Haw-Jyh | 60809-0101 |
| 09/352,142 **ABANDONED** | July 13, 1999 | Design Layout Migration Tool | Modarres, Hossein | 60809-0102 |
| 09/484,431; 6,574,759 | January 18, 2000; June 3, 2003 | Method For Verifying and Improving Run-Time of a Memory Test | Woo, Steven Cameron | 60809-0103 |
| 09/457,155 | December 8, 1999 | Memory System With Channel Multiplexing of Multiple Memory Devices | Garrett, Jr. Billy Wayne | 60809-0104 |
| 09/531,124 | March 17, 2000 | Compliant Semiconductor Package | Haba, Belgacem | 60809-0105 |
| 09/568,424; 6,545,875 | May 10, 2000; April 8, 2003 | Multiple Channel Modules and Bus Systems Using Same | Perino, Donald V. | 60809-0106 |
| 10/177,747; 6,657,871 | June 20, 2002; December 2, 2003 | Multiple Channel Modules and Bus Systems Using Same | Perino, Donald V. | 60809-0108 |
| 09/458,582; 6,643,752 | December 9, 1999; November 4, 2003 | Transceiver With Latency Alignment Circuitry | Donnelly, Kevin S. | 60809-0109 |
| 09/393,884; 6,640,292 | September 10, 1999; October 28, 2003 | System and Method For Controlling Retire Buffer Operation in a Memory System | Barth, Richard M. | 60809-0110 |

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|---|---|---|---|---|
| 09/401,977; 6,571,325 | September 23, 1999; May 27, 2003 | Pipelined Memory Controller and Method of Controlling Access to Memory Devices in a Memory System | Satagopan, Ramprasad | 60809-0111 |
| 10/101,243 | March 20, 2002 | Memory Module With Offset Data Lines | Garrett, Jr. Billy Wayne | 60809-0112 |
| 09/471,304 | December 23, 1999 | Integrated Circuit Device Having Stacked Dies and Impedance Balanced Transmission Lines | Perino, Donald V. | 60809-0113 |
| 09/547,881 | April 12, 2000 | Programmable Timing Module | Yeh, Gon-Jong | 60809-0114 |
| 09/499,025 | February 7, 2000 | System and Method For Aligning Internal Transmit and Receive Clocks | Stark, Donald C. | 60809-0115 |
| 10/020,921 | December 19, 2001 | Push-Pull Output Driver | Nguyen, Huy M. | 60809-0116 |
| 60/343,905 | October 22, 2001 | Clock Phase Control Circuitry and Method For Generating Distinct Receive and Transmit Clocks For Multiple Data Pins of a Memory Controller | Perego, Richard E. | 60809-0118PV |
| 10/278,708 | October 22, 2002 | Phase Adjustment Apparatus and Method For a Memory Device Signaling System | Hampel, Craig E. | 60809-0118 |
| 10/282,531 | October 28, 2002 | Method and Apparatus For Fail-Safe Resynchronization With Minimum Latency | Zerbe, Jared L. | 60809-0119 |
| 10/346,859 | January 16, 2003 | Active Impedance Compensation | Liaw, Haw-Jyh | 60809-0122 |
| 10/359,061 | February 4, 2003 | Apparatus and Method For Topography Dependent Signaling | Horowitz, Mark A. | 60809-0124 |
| 10/366,865 | February 14, 2003 | Delay Locked Loop Circuitry For Clock Delay Adjustment | Donnelly, Kevin S. | 60809-0125 |
| 10/455,059 | June 4, 2003 | Adjustable Clock Driver Circuit | Best, Scott C. | 60809-0126 |

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|---|---|---|---|---|
| 10/662,204 | September 12, 2003 | Adaptive Impedance Output Driver | Nguyen, Huy M. | 60809-0127 |
| 10/369,301 | February 18, 2003 | Memory Controller With Power Management Logic | Tsern, Ely K. | 60809-0129 |
| 10/410,390 | April 8, 2003 | Semiconductor Package With a Controlled Impedance Bus and Method of Forming Same | Gamini, Nader | 60809-0130 |
| 10/446,880 | May 27, 2003 | Pipelined Memory Controller and Method of Controlling Access to Memory Devices in a Memory System | Satagopan, Ramprasad | 60809-0131 |
| 10/661,225 | September 12, 2003 | System and Method For Adaptive Duty Cycle Optimization | Nguyen, Huy | 60809-0132 |
| 10/661,862 | September 11, 2003 | Configuring and Selecting Duty Cycle For an Output Driver | Nguyen, Huy | 60809-0133 |
| 10/453,368 | June 2, 2003 | Method For Verifying and Improving Run-Time of a Memory Test | Woo, Steven Cameron | 60809-0135 |
| 10/135,222 | April 29, 2002 | Adaptive Signal Termination | Rajan, Suresh | 60809-0136 |
| 10/625,914 | July 22, 2003 | DRAM Core Refresh With Reduced Spike Current | Tsern, Ely K. | 60809-0137 |
| 10/684,618 | October 13, 2003 | Calibrated Data Communication System and Method | Zerbe, Jared L. | 60809-0138 |
| 10/663,572 | September 15, 2003 | Method and Apparatus For Performing Testing of Interconnections | Yeung, Philip | 60809-0139 |
| 10/700,655 | November 3, 2003 | Integrated Circuit With Timing Adjustment Mechanism and Method | Zerbe, Jared L. | 60809-0140 |
| 10/690,402 | October 20, 2003 | Memory System With Channel Multiplexing of Multiple Memory Devices | Garrett, Jr. Billy Wayne | 60809-0141 |
| 10/695,418 | October 27, 2003 | System and Method For Controlling Retire Buffer Operation in a Memory System | Barth, Richard M. | 60809-0142 |

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|---|---|---|---|---|
| 10/699,116 | October 31, 2003 | Transceiver With Latency Alignment Circuitry | Donnelly, Kevin S. | 60809-0143 |
| NOT YET ASSIGNED | December 18, 2003 | Power Control System for Synchronous Memory Device | Tsern, Ely K. | 60809-0146 |
| 10/731,718 | December 8, 2003 | Charge Compensation Control Circuit and Method For Use With Output Driver | Stark, Donald C. | 60809-0147 |
| NOT YET ASSIGNED | December 30, 2003 | Semiconductor Package with a Controlled Impedance Bus and Method of Forming Same | Gamini, Nader | 60809-0148 |
| 10/738,293 | December 16, 2003 | Expandable Slave Device System | Garlepp, Bruno W. | 60809-0149 |
| 10/742,247 | December 19, 2003 | Apparatus and Method For Topography Dependent Signaling | Horowitz, Mark A. | 60809-0152 |